ABSTRACT:

A DC-offset correction circuit (I1, Q1) for a low-IF or zero-IF receiver, comprises a DC-offset control loop (O1, O2) embodied by: a summing device (9-1, 9-2) having a signal path input (10-1, 10-2), a DC control input (11-1, 11-2), and a summing output (12-1, 12-2); and an offset determining means (15-1, 15-2) coupled between the summing output (12-1, 12-2) and the DC control input of the summing device (9-1, 9-2). The DC-offset correction circuit (I1, Q1) further comprises a DC blocking circuit (17-1, 17-2) coupled to the summing output (12-1, 12-2) of the summing device (9-1, 9-2) and having a DC blocking output (18-1, 18-2) for providing an offset corrected output signal. The DC-offset control loop (O1, O2) and the DC blocking circuit (17-1, 17-2) advantageously interact in correcting DC offset.

Sole fig.